Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A CMOS active pixel sensor (APS) transducer array for sensing an image, the array having a number of APS's arranged in columns and rows and the array being adapted to decimate the image by accessing output signals only from selected APS's in the array, comprising:

a power terminal ~~means~~ adapted to be connected to a power supply;

a ground terminal ~~means~~ adapted to be connected to ground;

~~means~~ a switching circuit adapted to ~~for~~ electrically connect~~connecting~~ only the selected APS's between the power terminal ~~means~~ and the ground terminal ~~means~~for energizing the selected APS's for a complete image sensing cycle.

2. (Currently amended) A transducer array as claimed in claim 1 wherein the ~~connecting means~~switching circuit comprises:

a switch ~~means~~ for connecting the selected APS's to the power terminal ~~means~~; and

~~coupling means~~a coupler for connecting the APS's to the ground terminal ~~means~~.

3. (Original) A transducer array as claimed in claim 2 wherein the selected APS's are located in an array column.

4. (Original) A transducer array as claimed in claim 2 wherein the selected APS's are located in an array row.

5. (Original) A transducer array as claimed in claim 2 wherein the selected APS's are located in columns and rows of the array.

6. (Original) A transducer array as claimed in claim 2 wherein the selected APS's comprise all of the APS's located in selected array columns.

7. (Original) A transducer array as claimed in claim 2 wherein the selected APS's comprise all of the APS's located in selected array rows.

8. (Currently amended) A transducer array as claimed in claim 1 wherein the ~~connecting~~

~~means~~switching circuit comprises:

a switch ~~means~~ for connecting the selected APS's to the ground terminal ~~means~~; and

~~coupling means~~a coupler for connecting the APS's to the power terminal ~~means~~.

9. (Original) A transducer array as claimed in claim 8 wherein the selected APS's are located in an array column.

10. (Original) A transducer array as claimed in claim 8 wherein the selected APS's are located in an array row.

11. (Original) A transducer array as claimed in claim 8 wherein the selected APS's are located in columns and rows of the array.

12. (Original) A transducer array as claimed in claim 8 wherein the selected APS's comprise all of the APS's in selected array columns.

13. (Original) A transducer array as claimed in claim 8 wherein the selected APS's comprise all of the APS's located in selected array rows.

14. (Currently amended) A CMOS active pixel sensor (APS) transducer array for sensing an image, the array having a number of APS's arranged in N columns and M rows and the array being adapted to decimate the image by accessing output signals only from selected APS's comprising:

a power terminal adapted to be connected to a power supply;

a ground terminal adapted to be connected to a ground;

~~means for coupling~~a switching circuit adapted to selectively connect the APS's between the power terminal and the ground terminal, wherein the selected APS's are energized for a complete image sensing cycle, comprising:

- N transistor ~~means~~ switches wherein each of the N transistor ~~means~~ switches is connected between APS's in a respective column and the power terminal; and
- ~~further coupling means~~a coupler for ~~coupling~~ connecting the APS's in the respective columns to the ground terminal.

15. (Currently amended) A transducer array as claimed in claim 14 wherein the ~~further coupling means~~coupler comprises M transistor ~~means~~ switches, wherein each of the M transistor ~~means~~ switches is connected between APS's in a respective row and the ground terminal.

16. (Currently amended) A transducer array as claimed in claim 15 comprising a controller~~control means~~ coupled to the N and M transistor ~~means~~ switches for selectively activating ~~and~~ or deactivating the N and M transistor ~~means~~switches for the complete image sensing cycle.

17. (Currently amended) A CMOS active pixel sensor (APS) transducer array for sensing an image, the array having a number of APS's arranged in N columns and M rows and the array being adapted to decimate the image by accessing output signals only from selected APS's comprising:

- a power terminal adapted to be connected to a power supply;
- a ground terminal adapted to be connected to a ground ;
- ~~means for coupling~~ a switching circuit adapted to selectively connect the APS's between the power terminal and the ground terminal, wherein the selected APS's are energized for a complete image sensing cycle, comprising:
  - N transistor ~~means~~ switches wherein each of the N transistor ~~means~~ switches is connected between APS's in a respective column and the ground terminal; and
  - ~~further coupling means for coupling~~a coupler for connecting the APS's in the respective columns to the power terminal.

18. (Currently amended) A transducer array as claimed in claim 17 wherein the ~~further coupling means~~coupler comprises M transistor ~~means~~ switches, wherein each of the M transistor ~~means~~ switches is connected between APS's in a respective row and the power terminal.

19. (Currently amended) A transducer array as claimed in claim 18 comprising a controller ~~control means~~ coupled to the N and M transistor ~~means~~ switches for selectively activating ~~and~~ or deactivating the N and M transistor ~~means~~switches for the complete image sensing cycle.

20. (Currently amended) A CMOS active pixel sensor (APS) transducer array for sensing an image, the array having a number of APS's arranged in N columns and M rows and the array being adapted to decimate the image by accessing output signals only from selected APS's comprising:

- a power terminal adapted to be connected to a power supply;
- a ground terminal adapted to be connected to a ground;
- ~~means for coupling~~a switching circuit adapted to selectively connect the APS's between the power terminal and the ground terminal, wherein the selected APS's are energized for a complete sensing cycle, comprising:
  - M transistor ~~means~~ switches wherein each of the M transistor ~~means~~ switches is connected between APS's in a respective row and the power terminal; and

- ~~further coupling means for coupling~~a coupler for connecting the APS's in the respective row to the ground terminal.

21. (Currently amended) A transducer array as claimed in claim 20 comprising ~~control means~~a controller coupled to the M transistor ~~means~~ switches for selectively activating ~~and~~ or deactivating the M transistor ~~means~~switches for the complete image sensing cycle.

22. (Currently amended) A CMOS active pixel sensor (APS) transducer array for sensing an image, the array having a number of APS's arranged in N columns and M rows and the array being adapted to decimate the image by accessing output signals only from selected APS's comprising:

- a power terminal adapted to be connected to a power supply;
- a ground terminal adapted to be connected to a ground;
- ~~means for coupling~~a switching circuit adapted to selectively connect the APS's between the power terminal and the ground terminal, wherein the selected AP'S are energized during a complete image sensing cycle, comprising:
  - M transistor ~~means~~ switches, wherein each of the M transistor ~~means~~ switches is connected between APS's in a respective row and the ground terminal; and
  - ~~further coupling means~~a coupler for connecting ~~for coupling~~ the APS's in the respective row to the ground terminal.

23. (Currently amended) A transducer array as claimed in claim 22 comprising ~~control means~~a controller coupled to the M transistor ~~means~~ switches for selectively activating ~~and~~ or deactivating the M transistor ~~means~~switches for the complete image sensing cycle.

24. (Currently amended) In a CMOS active pixel sensor (APS) transducer array having a number of APS's arranged in columns and rows ~~and~~ adapted to be connected to a power supply, for providing output signals representing an image and wherein the outputs of selected APS's are ~~not~~ accessed to decimate the image thereby reducing the output bandwidth of the transducer array, a method of controlling power consumption in the array comprising the steps of:

a. determining the selected APS's having outputs that are to be ~~not~~ accessed;

b. connecting the selected APS's to the power supply for a complete image sensing cycle; and

~~b.~~c. disconnecting the ~~selected~~ APS's that are not selected from the power supply for the complete image sensing cycle.

25. (Original) The method as claimed in claim 24 wherein the selected APS's are located in predetermined columns.

26. (Original) The method as claimed in claim 25 wherein the selected APS's are located in predetermined rows.

27. (Original) The method as claimed in claim 24 wherein the selected APS's are located in every second, second to fourth or second to eighth columns.

28. (Original) The method as claimed in claim 24 wherein the selected APS's include all of the APS's located in predetermined columns.

29. (Original) The method as claimed in claim 28 wherein the selected APS's include all of the APS's located in predetermined rows.

30. (Original) The method as claimed in claim 24 wherein the selected APS's include all of the APS's located in predetermined rows.